

What Is Claimed Is:

- Sub 1*
1. A controller for microprocessor input/output to at least one external device, said controller comprising:
- 5 control logic;
- an Input/Output (I/O) crossover-switching network having a plurality of parallel pins;
- at least one serial I/O shifter in communication with said I/O crossover-switching
- 10 network, said at least one serial I/O shifter having at least one channel;
- a clock signal for clocking a transfer of serial data from said controller to the external device;
- 15 a latch signal for delimiting boundaries of transferred serial data;
- primary and secondary I/O signal pathways controlled by said I/O crossover-switching network for selecting I/O signals and usage of said plurality of
- 20 parallel pins for communication with and control of the external device; and
- wherein for said at least one channel, a first signal pathway is selectable between at least said primary signal pathway and said secondary signal
- 25 pathway for connection to said at least one serial I/O shifter.
2. The controller as claimed in claim 1 further comprising:
- optional signal pathways controlled by said
- 30 I/O crossover-switching network for selecting I/O signals and usage of said plurality of parallel pins

for communication with and control of the external device; and

wherein for said at least one channel, a second signal pathway is selectable between at least said primary signal pathway and said optional signal pathway for connection to a pin on the external device, said primary signal pathway being available to either said first signal pathway or said second signal pathway.

3. The controller as claimed in claim 1 further comprising an external source for said clock and latch signals.

4. The controller as claimed in claim 1 wherein said serial I/O shifter further comprises a high-speed serial shifter wherein serial data is transferred out of said shifter on one edge of said clock signal and transferred to said external device on the following edge of said clock signal.

5. A method for serializing parallel data comprising the steps of:

sampling selected parallel I/O signals with a serial I/O shifter;

selecting a signal path from a primary, secondary or optional signal path;

serially transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal;

asserting a latch signal for enabling an external device; and

outputting data as parallel I/O signals.

6. The method as claimed in claim 5 wherein said step of serially transferring bits of the data stream further comprises serially transferring bits at a rate of one bit per cycle of a clock signal.

5 7. The method as claimed in claim 5 wherein said step of sampling selected parallel I/O signals further comprises sampling selected parallel I/O signals on the leading edge of a latch signal to create a bit data stream.

10 8. The method as claimed in claim 5 wherein said step of outputting data further comprises setting a resolution of the parallel I/O signals using a frequency of the latch signal.

15 9. The method as claimed in claim 5 wherein said step of serially transferring bits further comprises serially transferring bits out of the serial I/O shifter on one edge of the clock signal; and

20 transferring bits from said I/O shifter to said external device on the following edge of the clock signal.

10. A method for parallel reconstruction of a serial data stream comprising the steps of:

25 selecting a signal path from a primary, secondary or optional signal path;

serially transferring bits of the data stream from an I/O multiplexer to an external device;

reconstructing the serial data into parallel I/O signals in a serial I/O shifter;

outputting the parallel I/O signals to an I/O crossover-switching network; and

asserting a latch signal for enabling another transfer of serial data from the external
5 device.

11. The method as claimed in claim 10 wherein said step of serially transferring bits of the data stream further comprises serially transferring bits at a rate of one bit per cycle of a clock signal.

10 12. The method as claimed in claim 10 wherein said step of outputting data further comprises setting a resolution of the parallel I/O signals using the number of serial bits transferred, clock speed and the assertion of a latch signal.

15 13. The method as claimed in claim 10 wherein said step of serially transferring bits further comprises serially transferring bits out of the serial I/O shifter on one edge of the clock signal; and

20 transferring bits from said I/O shifter to said external device on the following edge of the clock signal.